IN THE CLAIMS

Please amend the claims as follows:

Claims 1-54 (Canceled).

Claim 55 (Currently Amended): ~~The~~ A semiconductor device ~~according to claim 54,~~ comprising:

a semiconductor substrate;

a memory cell having a first channel and a first gate insulating film formed on the semiconductor substrate, the first gate insulating film comprising multiple layer films including a charge storage layer;

first shallow trench isolation regions formed in trenches provided in the semiconductor substrate, the memory cell being sandwiched between the first shallow trench isolation regions;

a transistor having a second channel and a second gate insulating film formed on the semiconductor substrate; and

second shallow trench isolation regions formed in trenches provided in the semiconductor substrate, the transistor being sandwiched between the second shallow trench isolation regions;

wherein the first shallow trench isolation regions have first concave portions on upper ends thereof;

wherein the second shallow trench isolation regions have second concave portions on upper ends thereof,

wherein an entire extent of the first concave portions are formed above the charge storage layer,

wherein a film thickness of the first gate insulating film at a central portion of the first channel and at portions contacting with the first shallow trench isolation regions are equal,

wherein a film thickness of the second gate insulating film at a central portion of the second channel and at portions contacting with the second shallow trench isolation regions are equal, and

wherein heights, from a surface of the semiconductor substrate, of upper surfaces of the first shallow trench isolation regions are higher than heights, from the surface of the semiconductor substrate, of upper surfaces of the second shallow trench isolation regions.

Claim 56 (Currently Amended): The semiconductor device according to claim ~~54~~ 55,

wherein the first gate insulating film includes a first insulating film as the charge storage layer comprised of silicon and nitrogen as main constituent elements thereof, a second insulating film formed on the first insulating film, the second insulating film comprised of silicon and oxygen, and a third insulating film formed between the first insulating film and the semiconductor substrate, the third insulating film comprised of silicon and oxygen, and

wherein a film thickness of the second insulating film at a central portion of the first channel and at portions contacting with the first shallow trench isolation regions are equal.

Claim 57 (Currently Amended): The semiconductor device according to claim ~~54~~ 55,

wherein the memory cell has a first gate electrode and the transistor has a second gate electrode, and

wherein the first gate electrode and the second gate electrode comprise polycrystalline silicon films, which are doped with impurities of conductivity types opposite to each other.

Claim 58 (New): The semiconductor device according to claim 55, wherein each of the first shallow trench isolation regions includes a first insulating filler,

wherein each of the second shallow trench isolation regions includes a second insulating filler,

wherein the upper surface of the first shallow trench isolation regions is the upper surface of the first insulating filler, and

wherein the upper surface of the second shallow trench isolation regions is the upper surface of the second insulating filler.

Claim 59 (New): A semiconductor device comprising:

a semiconductor substrate;

a memory cell having a first channel and a first gate insulating film formed on the semiconductor substrate, the first gate insulating film comprising multiple layer films including a charge storage layer;

first shallow trench isolation regions formed in trenches provided in the semiconductor substrate, the memory cell being sandwiched between the first shallow trench isolation regions;

a transistor having a second channel and a second gate insulating film formed on the semiconductor substrate; and

second shallow trench isolation regions formed in trenches provided in the semiconductor substrate, the transistor being sandwiched between the second shallow trench isolation regions;

wherein the first shallow trench isolation regions have first concave portions on upper ends thereof,

wherein the second shallow trench isolation regions have second concave portions on upper ends thereof,

wherein an entire extent of the first concave portions are formed above the charge storage layer,

wherein a film thickness of the first gate insulating film at a central portion of the first channel and at portions contacting with the first shallow trench isolation regions are equal,

wherein a film thickness of the second gate insulating film at a central portion of the second channel and at portions contacting with the second shallow trench isolation regions are equal,

wherein the memory cell has a first gate electrode and the transistor has a second gate electrode, and

wherein the first gate electrode and the second gate electrode comprise polycrystalline silicon films, which are doped with impurities of conductivity types opposite to each other.

Claim 60 (New): The semiconductor device according to claim 59,

wherein the first gate insulating film includes a first insulating film as the charge storage layer comprised of silicon and nitrogen as main constituent elements thereof, a second insulating film formed on the first insulating film, the second insulating film comprised of silicon and oxygen, and a third insulating film formed between the first insulating film and the semiconductor substrate, the third insulating film comprised of silicon and oxygen, and

wherein a film thickness of the second insulating film at a central portion of the first channel and at portions contacting with the first shallow trench isolation regions are equal.